Oral Abstracts

Semiconductor Technology for Ultra Large Scale Integrated Circuits and Thin Film Transistors III

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IT's a 3D world - Challenges and opportunities for 3D logic and memory ULSI devices

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As dimensional scaling becomes increasingly challenging, continued functionality gains can be achieved by packing more devices per unit volume, i.e., adding a third dimension. This scaling is a paradigm shift since it is not scaling in the traditional sense, but provides opportunities for continued increase in device density at chip level, chip density at package level and package density at system level. All this effort towards scaling along the third dimension allows a relaxation in the cost and technical pressures of traditional two dimensional scaling, while continuing to provide systems that pack ever more functionality. For memory technologies, charge trap flash transistors are likely to be the first embodiment of this approach, as exemplified by announcements from Samsung and Toshiba. However, the real gain may be from moving to simpler cross point Resistive RAM devices where such device level stacking becomes easier to implement. While this offers the promise of simple yet dense memories, there are quite a few challenges to overcome, such as reliable storage, retention and endurance. Another approach that is actively under consideration is 3D stacking of memory chips. Such homogeneous stacking of chips using through Silicon via (TSV) technologies helps to not only increase package level memory density, but addresses latency issues for high speed high data rate system needs. Logic technologies suffer from high leakage , both off state and on state. Employing a 3D ? Will better turn-off helps characteristics of FETs. However, challenges, such as lowering parasitic R and C along with cost and ease of manufacturability, must be considered. Finally, for true impact, it is important to deliver performance gains at the system level, such as encompass multiple functional blocks on the same die system on a chip (SOC). However, the gains from SOC are off-set by design, process, integration challenges and potential yield losses in high volume manufacturing. A parallel and complementary path being pursued involves stacking traditionally incompatible technologies like CMOS logic, memory, analog, MEMS, photonics, RF chips in the same package using 3D TSV interconnects. Such heterogeneous stacking architectures enable many new applications.

Semiconductor technology evolution for ULSIC

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Recently, semiconductor industry has been facing extreme difficulties, both in memory and logic, to keep maintaining the beauty of sharing the benefit of the scaling between manufacturer as a supplier and system maker as a user. Scaling limitations are originated from various aspects: patterning capability, reliability, power, performance, yield, and cost. As one of the potential solutions, an adaptation of 3-dimensional structure is intensively investigated, for example, vertical channel transistor in DRAM, monolithic stacking of NAND cells in flash, and FinFET approach in Logic. In this presentation, some of Samsung's perspective on these challenges and recent development activities will be shared.

Nanoscale metal silicides

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As the integrated circuits (IC) industry moves into the nano era, scaling down the metal silicide contacts and gates have become an important issue. Many efforts with the bottom-up approach have been made to fabricate nanoscale silicdes without elaborate microlithography. As opposed to zero-dimensional nanocrystals, metallic nanowires (NWs) can act both as interconnects for the transport of charge carriers as well as active device elements.

The early focus on the study of epitaxial silicide NWs has been on the rare-earth/Si systems, based on the anisotropic lattice mismatch between silicides and Si substrates. Subsequently, the NW growth in isotropic systems was found to proceed via the formation of a twinned structure to break the symmetry of the interface and lead to the asymmetric growth of epitaxial $CoSi_2$ and $NiSi_2$ NWs. The use of nitride-mediated epitaxy method effectively diminished the flux of metal atoms and allowed sufficient time for the strain to be released by means of shape transition during the epitaxial growth of a number of silicide NWs at elevated temperatures. In addition, a large number of free-standing silicide nanowires has been grown by a variety of methods. Silicide/Si/silicide nanowire heterostructures were fabricated.

In this talk, recent progress in the investigations on silicide nanowires will be presented. Examples will be given on the following topics: 1. growth of Ti, Co, Ni and Ta silicide nanowires by a vapor condensation method, 2. in situ growth of self-assembled $TiSi_2$ silicide nanowires in an ultrahigh vacuum transmission electron microscope, 3. in-situ control of atomic-scale Si layer with huge strain in the nano-heterostructure NiSi/Si/NiSi through point contact reaction, 4. single crystalline PtSi nanowires, PtSi/Si/PtSi nanowire heterostructures and nanodevices, 5. in–situ TEM observation of repeating events of nucleation in epitaxial growth of Nano $CoSi_2$ in nanowires of Si and 6. homogeneous nucleation of epitaxial $CoSi_2$ and NiSi in Si nanowires.

Silicon grow-in-place nanowires and their applications

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Our group has introduced the grow-in-place approach for creating horizontally arrayed Si nanowires (NWs). In the grow-in-place technique, horizontal NWs are grown on the substrate of final use thereby avoiding the usually employed grow, pick, and place steps. Applications for these Si nanowires include use as ultra-fine probes for sensing, ultra-fine probes for monitoring, and NW thin film transistors.

Grow-in-place Si NWs are produced by using a growth template, a catalyst, and the vapor-liquid solid (VLS) technique. In the grow-in-place approach, the VLS catalyst is positioned in the growth template. The resulting nanowires can be kept within the template or allowed to extrude. The former has the advantage that NWs can be controlled to be poly-crystalline or single crystal, as needed, and are exactly positioned facilitating subsequent processing such as TFT fabrication and subsequent array arrangement. The extruded version has the advantage that subsequent processing is done on exposed wires but the disadvantage of imprecise positioning. The fabrication of both types of grow-in-place silicon nanowires, modification of their properties, and their applications will be discussed.

In-plane silicon nanowires for field effect transistor applications

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Low temperature plasma process have allowed the development of a-Si:H based TFTs for large area electronics. Further, the crystallization of this material by various processes as well as the direct deposition of polycrystalline silicon films has been studied in order to overcome the limitations of a-Si:H TFTs (low mobility and threshold voltage shift), which do not make them suitable for integrated circuits. After a short review on the past developments in this area, we will move to a new process based on the realization of silicon of nanowires (SiNWs), which can fulfill the requirements of large area deposition and high device performance. Indeed, silicon nanowires have attracted much attention. However, the inegration of SiNWs, usually produced by VLS, is a challenging issue for scaling up the SiNWs functionalities in a mainstream planar CMOS architecture. We have recently proposed and demonstrated the planar growth of SiNWs via an in-plane solid-liquid-solid (IPSLS) method, which is intrinsically compatible to the mainstream planar CMOS technology. During an IPSLS process, the liquid catalyst (indium) drops absorb an a-Si:H and transform it into well-defined crystalline SiNWs.[1] The morphology and the growth position/orientation of the SiNWs arrays can be effectively controlled. We show that the guided growth of the in-plane SiNWs can be conveniently realized during the growth of SiNWs by predefined simple step-edge lines, without any lithography resolution limit.[2] This enables an all-in-situ integration of self-aligned SiNWs field effect transistor (SiNWs-FET) arrays. We found that the incorporation of indium catalyst atoms in the crystalline SiNWs leads to effectively p-doping in the SiNWs. The SiNWs-TFT units realized in a simple bottom gate structure show a promising hole mobility of 70-228 cm2/vs with on/off ratio >103. This in-situ position strategy will lay an important basis for direct device integration of various SiNWs-based sensor and transistor applications.

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[2] L. Yu et al., Appl. Phys. Lett. 95, 113106 (2009).

Application of graphene and carbon nanotubes to transistors and interconnects

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Improvement in LSI performance by miniaturization is becoming more and more difficult. We are trying to employ nano-carbon materials, such as graphene and carbon nanotubes (CNTs), as channel and interconnect materials to realize low power-consumption LSIs without relying on miniaturization. In this presentation, we will talk about our recent progress on the application of graphene to transistor channels. Graphene synthesis on a 200-mm Si wafer by chemical vapor deposition (CVD) and electrical properties of CVD-graphene transistors will be described. Especially, details of graphene growth on Cu film, such as nucleation of graphene islands depending on the growth condition, will be explained. We will also talk about CNT interconnects, which have been studied at Fujitsu and MIRAI-Selete for years. Special emphases will be placed on the fabrication process of CNT vertical interconnects and their reliability.

The graphene-related work was partly supported by the Japan Society for the Promotion of Science (JSPS) through its Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program).

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Keynote: Unipolar CMOS logic for post-Si ULSI and for TFT technologies

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It has become increasingly difficult to scale down Si-based CMOS transistors for ULSI applications, and high-mobility channel materials are being seriously considered as alternatives to Si for future generations of CMOS technology. Among the leading contenders are carbon nano-tube, graphene, and a few III-V semiconductors, although only III-V semiconductors have a realistic chance of succeeding Si within a decade, according to this author's assessment.

The high carrier mobilities in aforementioned materials are often associated with their small effective masses, which may give rise to lower densities of states, and thus fewer carriers in the conduction channel for a given gate voltage. Therefore, an undesired consequence of the lower density-of-state is to reduce the advantage of high carrier mobility in enhancing the drive current. As a result, it is not obvious whether a high-mobility channel does indeed lead to high drive current. This question has been addressed for a few high-electron-mobility III-V semiconductors, and the results are quite encouraging.

A major issue one must deal with is the very low hole mobility in many high-electron-mobility III-V semiconductors, which limits the speed of the p-channel transistor and slows down the entire CMOS logic circuit, despite the high electron mobility in the n-channel transistor. A novel 'unipolar' CMOS logic, which does not need a p-channel transistor in the CMOS switch, will be introduced to overcome this problem.

The 'unipolar' CMOS concept can also be applied to many TFT materials, such as amorphous Si, ZnO, and numerous organic semiconductors, where it is either difficult to incorporate both p-type and n-type dopants in the same material, or there is a very large disparity between electron and hole mobility.

Epitaxial techniques for semiconductor manufacturing

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Epitaxial techniques for semiconductor manufacturing are on a path to higher sophistication and more challenging requirements while there is increased concern about the cost and affordability of these processes. In particular, capabilities needed for Si-based epitaxial material deposition are changing rapidly. One aim of this presentation is to provide a view of approaches used in the Si-based epitaxy for others from outside this space. The second aim of the presentation is to provide a framework for discussions with experts from the TFT space, to seed learning of methods developed to obtain higher performance at reasonable cost on large-scales

Electron and hole trapping in polycrystalline and amorphous oxides for novel CMOS devices

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Understanding the interplay between electrons and defects in polycrystalline and amorphous oxides is important for improving the performance of novel CMOS devices. We model the electronic structure and spectroscopic properties of electron and hole states as well as oxygen vacancies and impurities in ZrO_2, HfO_2, amorphous SiO_2, as well as at the $HfO_2/SiO_2/Si$ interfaces and at grain boundaries of polycrystalline HfO_2. Our periodic and embedded cluster calculations use DFT and a hybrid density functional and accurately predict band gaps of materials and the electronic structure of interfaces. They demonstrate the wealth of polaronic behavior in m-HfO_2 and in closely-related systems, including negatively charged oxygen vacancies in m-HfO_2 and electron and hole trapping (electron polaron, Hf^{3+}, and hole polaron, O^-) in perfect m-HfO_2 lattice. We investigate the properties of grain boundaries and impurities in polycrystalline HfO_2 using a multi-scale approach linking atomistic calculations, periodic DFT and an embedded cluster method. We demonstrate that migration of O-vacancies and their eventual segregation at the GB can lead to the formation of a conductive sub-band within the dielectric energy gap. The injected electrons captured by the GB defects are effectively transported through the percolation path along the GB. Electron trapping/detrapping by the GB vacancies can be responsible for the high-low current switching observed in capacitor structures. These results also suggest that the breakdown filament in HfO_2 films may preferentially form along GBs. We predict the geometric and electronic structures and spectroscopic properties of doubly ionized and negatively charged oxygen vacancies in a-SiO_2 and demonstrate that negatively charged vacancies serve as deep electron traps. The results of our calculations significantly widen the range of defect states originating from the polycrystalline structure, oxygen deficiency and disorder of bulk oxides and thin gate oxide layers and considerably increase the number of potential inter-conversion processes.

Zinc oxide-based transparent TFTs produced at low temperature

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Metal oxide materials have emerged as a competitor to thin-film silicon and organic materials for thin-film transistors (TFTs) over the past few years. Although there have been several reports of excellent n-type operation with mobility in excess of 50cm2 V-1 s-1 and on-off ratios of greater than 107 metal oxides still present many engineering challenges. In particular the interface between the channel semiconductor and the gate dielectric has a significant effect upon TFT characteristics. If metal oxides are to address large area electronic applications then it is necessary to have a semiconductor channel and gate dielectric material that can both be produced at a sufficiently low temperature for a low cost substrate to be employed. This paper will describe our work on the use of a novel high target utilisation sputtering (HiTUS) system to deposit a range of semiconducting channel materials and metal oxides at temperatures compatible with the use of plastic substrates. A series of TFTs with a range of semiconductor and dielectric combinations have been manufactured and their operation and stability will be discussed .

High performance a-IGZO TFT and TFT circuits for display application

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Amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistors (TFTs) are of increasing interest due to their excellent characteristics, such as field-effect mobility of >30 cm2/V s, low threshold voltages <5 V and good uniformity. Since a-IGZO TFTs exhibit superior characteristics over organic or a-Si:H TFTs, a-IGZO TFT technology has been improved rapidly towards the realization of TFT backplanes for advanced active-matrix displays. Moreover, a-IGZO can be deposited by reactive sputtering, which make it possible to change the current TFT production line based on hydrogenated amorphous silicon (a-Si:H) to oxide based active-matrix backplane line for next-generation displays. In addition, low processing temperature makes a-IGZO devices compatible with flexible substrates such as plastic. The parasitic capacitance, known as the gate-to-drain capacitance (Cgd), is proportional to the overlap area, which is the cause of kickback/feed-through voltage and higher noise and lag in the devices using the TFTs as switching elements. Therefore, we developed self-aligned a-IGZO TFT and coplanar TFT having very low parasitic capacitance using bottom gate and top gate structures. The self-aligned a-IGZO TFT with 2 瘦 overlap length exhibits a saturation field-effect mobility of 42.59 cm2/Vs and the ring oscillator made of the a-IGZO TFTs shows excellent switching speed. The inverter, ring oscillator, level shifter, DC-DC converter and shift resistor made of a-IGZO TFTs will be discussed according to the device structure.

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2. D. Geng, D.H. Kang and J. Jang IEEE EDL, 2011, in press

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Comparative analysis of organic thin film transistor structures for flexible E-paper and AMOLED displays

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Organic thin-film transistors (OTFTs) have attracted considerable attention owing to their potential applications in flexible e-paper and active matrix organic light-emitting diode (AMOLED) displays. The bottom-contact device structures include bottom-contact top-gate (BCTG) and bottom-contact bottom-gate (BCBG) have been popularly employed for circuit integration of OTFTs in display backplanes because of the process difficulty of making source/drain metal onto the organic semiconductor layer with precise patterning. When OTFTs are used in the display backplane, the pixel electrode, which connects the bottom electrode of the display media to the drain or source of the switch OTFT in the e-paper display, and the driving OTFT in the AMOLED display, will form parasitic effects with the OTFTs. In this work, the parasitic effects in both BCBG and BCTG structure based OTFT backplanes will be carefully investigated and compared. It is found that, in BCBG structure OTFT backplane, the presence of the pixel electrode may result in shift of the transfer characteristics and significant decrease of output impedance. The results are considered to be acceptable for driving e-paper displays with increasing the gate switching voltage swing. But for AMOLED display applications, very thick interlayer is needed to be used to suppress the parasitic effects, which, however, may increase the process cost and difficulty. Although BCTG OTFTs are not sensitive to the parasitic effect due to the presence of the pixel electrode, but can cause larger parasitic capacitance between the gate and the pixel electrode (electrically connected to the drain of the OTFT), which needs to be considered in the design to reduce the feed-through voltage for switch OTFTs.

Structural characteristics of transition metal oxides enabling resistive memory operations

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Resistance change memory (RRAM) based on transition metal oxides, which can switch between high and low resistance states by changing the resistivity of a conductive filament in the dielectric, has attracted attention due to its promise of high density, speed, and retention. While progress had been made in identifying key factors driving the metal oxide switching, there is no sufficiently developed microscopic description of the conductive filament features that enable memory operations. By combining electrical, physical and transport/atomistic modeling results we discuss relationship between RRAM switching and nanoscale conductive filament properties. Characteristics of the reset/set operations, described in terms of oxidation/reduction processes assisted by both temperature and electric field, are found to be determined by the properties of the oxygen-deficient conductive filament. The essentially non-uniform filament shape, which is controlled by the power dissipation along the conductive path across the dielectric during the forming process, determines temperature and electric field profiles during the device switching and, consequently, the resistivity of the memory cell in its high and low resistive states. An atomic-level understanding of the conductive filament properties allows for engineering the memory cell operating in a low-power regime.

Nonvolatile memories for nano and giga electronics applications

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The development trends of ULSICs and TFTs are on the opposite directions. The former is toward squeezing nano-size devices into a small die; the latter is toward expanding the panel size to the extremely large dimension. In spite of the difference, basic device operation principles in both technologies are the same, i.e., the field effect transistor. Memory functions in ULSICs have been constantly advanced with the improvement of the logic functions. Traditionally, memory functions are rarely considered in the TFT field due to the focused application to the pixel-level liquid crystal driving. In this talk, recent developments in the memory area will be discussed. For the ULSIC field, new nanocrystals embedded high-k dielectric nonvolatile memories including device performance and reliability will be presented. This kind of device is critical to the next generation IC products. For the TFT area, the new floating-gate a-Si:H TFT nonvolatile memory device characteristics will be shown. This kind of device will expand the function and performance of future LCD and non-LCD products. General challenges of semiconductor memory technologies will be discussed.

Understanding the switching mechanism in RRAM devices and the dielectric breakdown of ultrathin high-k gate stacks from first principles calculations

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RRAM devices received increased interest lately as advanced non-volatile memory technologies in terms of low operating power, high density, better non-volatility, fast switching speed, and compatibility with conventional CMOS process. However, up to date the fundamental physical principles controlling the switching are not well understood. I will present our recent first-principles simulations based on density functional theory (DFT) to elucidate the effect of oxygen vacancy defects on the electronic structure of rutile TiO2 and NiO using the local density approximation with correction of on-site Coulomb interactions (LDA+U). I will discuss the vacancy filament induced defect states within the band gap which can lead to the defect assisted electron transport and account for the on-state low resistance conduction in bulk rutile TiO2 and NiO. For CMOS devices on the other hand the reliability of the gate stack is becoming a significant challenge with the continuous scaling of transistors, due to the ultrathin oxides and defects in the gate stack. The degradation of the gate oxides has been observed under electrical stress, due to traps generated by defects, e.g. oxygen vacancies present in these materials. First principles methods based on density functional theory and non-equilibrium Green □function calculation provide a physical model of the breakdown mechanism; the thermodynamic stability, defect trap energies and interface vacancy segregation probabilities are calculated, and the effect on the tunneling current of these oxygen vacancy configurations will be discussed.

Manipulation of graphene properties by interface engineering

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Graphene, a new allotrope of carbon, received a great deal of interest although it was discovered very recently. In contrast to traditional semiconductors, the unique two dimensional structure of graphene offers the necessity and possibility in studying the interface characteristics for its sensitivity to the top surface and interface between graphene and the substrate. We are thus interested in understanding graphene surface and interface issues in electronic structure, carrier transport and related phenomena down to nano-scale. In this presentation, we investigate the mechanisms of graphene interface coupling to different substrates and interacting with inert adsorbates, both experimentally and theoretically. At first, the crucial roles of the substrate (interfacial effects) played in graphene applications are meticulously interrogated. To suppress the deleterious substrate effect on graphene intrinsic electronic structure and carrier transport properties, we have modified the substrate by highly ordered SAMs. The charge transfer is unambiguously corroborated by KPFM and transport measurement results. The measured temperature dependence of resistivity provides the evident correlation between the transport characteristics and the phonon-electron scattering by the interplay between graphene and the substrate. After diminishing the unwanted scattering origins, a nearly one order of increase in mobility is obtained. Subsequently, through molecular self-assembly above graphene by organic molecules (surface effect), both n-type and p-type doped mechanically exfoliated graphene sheets are accomplished. By exploiting the Kelvin probe force microscopy (KPFM), the charge transfer process identified as the key issue is quantitatively analyzed by a self-consistent tight binding model. By combining the two techniques, graphene PN junction will be demonstrated if p-type and n-type regions are fabricated in a graphene sheet on the modified substrate. Moreover, the junction interface can be monitored by KPFM. The insightful understanding of graphene PN junction provides numerous opportunities in both novel electric and optoelectronic devices.

Short channel effects and drain field relief architectures in polysilicon TFTs

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Future system-on-panel applications require further performance improvement of circuits based on polysilicon TFTs. The biggest leverage in circuit performance can be obtained by reducing channel length from the typical, current values of 3-6 um to 1 um, or less. Therefore, short channel effects in scaled down polysilicon TFTs will have to be controlled in order to allow proper operation of the devices. In this work we review a number of specific aspects of the electrical characteristics of short channel devices (channel lengths down to 0.4 um). In particular, the following topics will be discussed: i) parasitic resistance effects; ii) kink effect; iii) threshold voltage roll off; iv) drain induced barrier lowering; v) electrical stability. Short channel effects and hot carrier induced instability in scaled down self-aligned (SA) polysilicon TFTs appear to be a serious issue and drain field engineering is mandatory. Indeed, lightly doped drain (LDD) architecture has been shown to improve short channel effects, although at the expenses of increased parasitic resistance. Series resistance can be substantially reduced in the gate overlapped LDD (GOLDD) structure, due to gate modulation of the LDD regions. However, gate-drain overlap capacitance represent a serious limitation in GOLDD architecture but can be minimized by adopting a fully SA process, using conductive sidewall spacers. In this work, we present a detailed study of short channel effects and hot carrier related instability in fully SA GOLDD TFTs with LDD extension of 0.35 um and different doping doses (from 0.6 to 2.5 1013 cm-2) with channel lengths down to 1 um. By comparing both conventional SA and fully SA GOLDD TFTs, we found that short channel effects can be mitigated and degradation of device characteristics can be substantially reduced in fully SA GOLDD structure. In addition, from the electrical characteristics we also identified optimal LDD doping concentration. Two-dimensional numerical simulations show that such improvements are mainly due to reduction of floating body effects.

The potential application of oxide thin film transistor for active matrix display

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Single-grain germanium TFTs

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Germanium (Ge) has been considered as an alternative channel material for both MOSFET and TFT due to the potentially higher electron and hole mobilities than Si. However, in the Ge MOSFET, the high interface states density at the Ge/insulator and the fast dopant diffusion into channel has limited performance, especially for the n-channel device. In the Ge TFTs, off current becomes very large due to carrier generation at grain boundaries in addition to the aforementioned two problems. In this report we will review our recent achievements in location-control of Ge grains and high performance single-grain (SG) Ge thin film transistor (TFT) fabricated inside the Ge grain. Amorphous Ge film was deposited on SiO2 with small cavities/Si substrate by DC magnetron sputtering. Large Ge grains having a grain size of 15 microns were obtained at predetermined positions by the Czochralski process using excimer-laser. Capping silicon dioxide was applied before the laser crystallization with which a high quality Ge/insulator interface was formed. Source and drain were fabricated by doped Si instead of the Ge counterpart, which suppresses the fast dopant diffusion in the channel. N- and p-channel SG Ge TFTs showed electron and hole mobility of 3337cm^2/Vs and 1719cm^2/Vs, respectively. On/off current ratio for the both types of TFTs was in the order of 10^7.

Source-gated transistors for versatile large area electronic circuit design and fabrication

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Source-gated transistors (SGTs) [1] are three terminal electronic devices comprising a potential barrier at the source which controls the current and in which the gate electrode lies opposite the source contact, overlapping it. The gate-induced electric field modulates the height of the source barrier and thus changes the current between source and drain. Important advantages over the conventional field-effect transistor (FET) are derived from this mode of operation: saturation at very low voltages for lower power dissipation and a diminished dependence of saturated drain current on drain field for high output impedance.

The paper describes how SGTs can be optimized for particular applications and for the characteristics of specific fabrication processes. Schottky-barrier SGTs can be integrated together with FETs and have been fabricated in thin-film a-Si:H [1] and poly-Si [2] and, more recently, in solution-processed single-crystal inorganic nanowires. The control of the source barrier via gate action can be applied to virtually any semiconductor material system, assuming a source barrier can be formed and the gate lies on the opposite side of the semiconductor from the source. It is shown how the saturation voltage can be made an order of magnitude smaller than in equivalent FETs for power savings of over 50% at the same current output. The SGT also achieves a better saturation regime, with lower output conductance over a larger range of drain voltages [2, 3].

It is expected that these performance characteristics can be optimized through device engineering to produce repeatable transistor behaviour in processes with large manufacturing tolerances, such as printing and large-area electronics with increased energy-efficiency or improved analog and mixed-signal performance. Flat-panel lighting, remote sensing and signal processing are some of the applications which could benefit from incorporating these devices.

SiGe, Ge and III-V materials and processes for beyond-Si CMOS and more-than-Moore applications

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Whereas VLSI evolution initially relied completely on CMOS dimensional area scaling, it has now become a playground for materials scientists since device engineers need more and more new materials to keep up with performance scaling demands. After the introduction of Cu/low-k in BEOL and high-k/metal gates and SiGe source/drains for strained Si channels in FEOL, one is heading now for new channel materials in the hunt for higher drive current. In this last area, germanium has got in the focal point since about 7-8 years, followed later on by compound semiconductors (III-V).

A few major obstacles however have to be overcome. First of all, the incompatibility of these materials with the mandatory Si substrate necessitate innovative epitaxial growth and integration approaches to overcome defects induced by the huge lattice mismatch and the polar nature of III-V. Next, these semiconductors ask for new gate dielectric materials as the well-proven recipes of Si-based oxides are not working for various reasons. The lack of a stable, high-quality native oxide for both semiconductors forces researchers to focus more on the interface rather than on the dielectric material itself. Ways how to resolve these issues will be discussed: deposition of Ge and III-V materials in regular STI isolation structures on large size wafers by selective epitaxy, manufacturing of GeOI and III-VOI by wafer bonding, deposition of high-k layers on these channel materials and interface passivation. We will also discuss how the choice of the transistor architecture helps overcoming some of these problems.

Overcoming these roadblocks however will not only allow to continue the ITRS roadmap for scaling beyond the 16 nm node, but generates at the same time opportunities beyond regular CMOS/VLSI technologies. Some examples: the low thermal budget of Ge MOSFET processing allows making these devices on other than Si substrates, e.g. on glass plates. On the other hand, the monolithic integration options for Ge and III-V layers leads very naturally to the construction of e.g. optical devices on Si substrates.

Electrical atomically controlled CVD processing for doping in future Si-based devices

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The concept of atomically controlled processing for future Si-based devices is based on atomic-order surface reaction control in Si-based CVD epitaxial growth. The final goal is the generalization of atomic-order surface reaction processes and the creation of new properties of Si-based ultimate small structures which will enable novel devices concepts [1-3]. Here we discuss the atomic layer processing approach for B and P doping in particular, considering dopant activation especially.

By ultraclean low-pressure CVD using SiH_4 and GeH_4 gases, high-quality low-temperature epitaxial growth of $Si_{1-x}Ge_x$ with atomically flat surfaces and interfaces on Si(100) is achieved [1]. Si-based epitaxial growth on B or P atomic layer formed on Si(100) or $Si_{1-x}Ge_x$(100) surfaces is achieved at below 500^oC. B doping dose of about $7x10^{14}$ cm^{-2} is confined within an about 1 nm thick region, but the sheet carrier concentration is as low as $1.7 x10^{13}$ cm^{-2} [4]. The in-situ B doping in tensile-strained Si epitaxial growth suggests that the low electrical activity is caused by B clustering as well as the increase of interstitial B atoms [5].

In unstrained Si cap layer growth on the P atomic layer formed on $Si_{1-x}Ge_x$(100) with the P atom amount below of about $4x10^{14}$ cm^{-2} using Si_2H_6 instead of SiH_4, the incorporated P atoms are almost confined within 1 nm around the heterointerface [6]. It is found that tensile-strain in the Si cap layer growth enhances P surface segregation and reduces the incorporated P amount around the heterointerface. Electrical inactive P atoms are generated by tensile-strain in heavy P doped region [7].

It was confirmed that band engineering for group IV semiconductors becomes possible by strain control of the $Si_{1-x}Ge_x$/Si heterostructure due to striped patterning and that heavy C atomic-layer doping suppresses strain relaxation as well as intermixing between Si and Ge at the $Si_{1-x}Ge_x$/Si heterointerface [2].

These results open the way for group IV semiconductors with high mobility as well as high carrier concentration by strain control for ULSIs using atomically controlled processing.

Physical modeling of charge transport and degradation in high-k stacks for logic device and memory applications

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The optimization of high-k stacks for future CMOS logic device technology requires to reduce tunneling currents and SILC, in order to both reduce the static power consumption and limit the reliability issues related to the high-k stack aging (i.e. breakdown). Furthermore, the operation principle of resistive switching memories (RRAM), considered a promising technology for next generation NVM devices, is based on the creation of conductive filaments (CF) in the high-k stacks, which is essentially a controlled dielectric breakdown. In this scenario, the understanding of the physical mechanisms governing the charge transport and the degradation of high-k stacks is crucial for improving the reliability of advanced CMOS high-k stacks and the reliability and operation of RRAM devices. Physics-based models describing charge transport, degradation and breakdown/forming processes in high-k dielectrics are strongly demanded in order to understand the key factors governing the degradation and breakdown of high-k dielectrics, the temperature-voltage dependencies of the leakage current, the statistics and the scalability limits of both RRAM devices and high-k stacks. We present in this paper a physical model reproducing accurately the charge transport and the degradation/breakdown processes in high-k stacks. The charge transport through high-k dielectrics is described through a multi-phonon Trap Assisted Tunneling (TAT) model. The CF formation occurring during forming/breakdown, which occurs through a temperature-driven positive-feedback process triggered by the current increase through the percolation path, is quantitatively described by including the local power dissipation, the temperature increase and the defect generation inside the high-k stacks. This model reproduces accurately the gate current measured across high-k stacks in static conditions and during the electrical stress experiments leading to the dielectric breakdown. Characteristics of defects assisting the charge transport are directly linked to the material properties, i.e. to O vacancy inside the high-k material. The model allows deriving the 3D maps of temperature and defect density inside the high-k material, thus providing quantitative insights into the features of the CF responsible of the resistance switching in RRAM devices and breakdown in gate stacks. The model is used also to evaluate the leakage current, the forming voltage and TDDB statistics.

Success in measuring the lowest off-state current of transistors in the world

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These days, research on TFTs using IGZO (IGZO TFTs) is popular. In particular, a technique for reducing power consumption by using low off-state current of IGZO TFTs has attracted attention in display fields. This time, we found that an IGZO TFT we fabricated has extremely low off-state current of the order of yA (*yoctoampere*). 'y (*yocto*)' is a SI prefix showing the smallest unit denoting a factor of 10^{-24}. Measurement of yA-level off-state current is reported for the first time.

In general, the amount of the off-state current of transistors is easily known by measuring the *Id-Vg* characteristics of transistors. However, the off-state current of our IGZO TFT is found to be lower than 10^{-13} A, the detection limit of the measurement instrument, even by increasing their channel widths as large as 1 m. Thus, a conventional measurement cannot find a correct value of off-state current.

Therefore, we measured the extremely low off-state current by estimating total amount of charge which flowed over time through an IGZO TFT with a channel width of 100,000 □m. We measured a voltage at a node with capacitance *C* for a long time, and then calculated the charge amount at the node *Q* as $Q = C \triangle V$. The off-state current was measured at constant temperature, under dry air (having a dew point of -60 degrees of Centigrade or lower) and dark conditions. In addition, the TFT had a gate-offset structure to reduce the capacitance *C* to about 70 aF/□m. As a result of measurement for 6 hours at 85 degrees of Centigrade, the voltage decreased by about 30 mV ($\triangle V$ = 30 mV). The result shows that the off-state current is about 100 yA/□m at 85 degrees Centigrade.

This time, we succeeded in fabrication of IGZO TFTs with yA-level off-state current. Such transistors can be applied to not only low-power displays but also low-power LSIs and memories in ULSI fields. We will continuously develop the memories using IGZO TFTs.

Self-heating issue of Poly-Si TFT on glass substrate

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One of critical issues of TFT for large scale integration is temperature rise of TFT due to self-heating. In this presentation, we would like to discuss about this issue. The experimental results to be presented is temperature rise of poly-Si TFT during operation. The temprature was evaluated by determining the thermal resistance from the temperature-dependent negative-drain conductance. TFTs are fabricated using a laterally-grown poly-Si film. By aligning TFT channel direction with the grain growth direction, effects of grain boundary on carrier transport becomes less significant so that direct evaluation of self-heating from drain characteristic becomes possible. SOI MOSFET is also investigated. Results indicate that the thermal resistance of TFT is 40 times as large as that of SOI MOSFET. As a consequence, tempreature rise of TFT reaches to 150 K even under normal operation condition. Heat dissipation path is also investigated by determining the thermal resistance of TFTs having various dimensions. Results clearly indicate that design of thermal path through the gate becomes of importance for TFTs. Effect of stripe channel on TFT performance and temperature rise is also discussed.

Bridged-grain TFT

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A new technique, bridged-grain (BG) TFT is introduced. Using this BG process, various low temperature polycrystalline silicon (LTPS) TFT devices can be improved. In this talk, we illustrate the use of BG using eximer laser annealed (ELA) poly-Si TFT. It is shown that grain boundary effects can be reduced. Important electrical properties such as sub-threshold swing, threshold voltage, maximum field effect mobility, leakage current, on-off ratio and device uniformity across the substrate can all be improved using this BG technique. The improvement can be achieved at low cost, thus making inexpensive, high performance LTPS TFT a reality.

Keynote: Recent advances on nano-materials for advanced packaging applications

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The advance of semiconductor technology is mainly due to the advances of materials, especially polymeric materials. These include the use of polymers as: resists(for deep submicron lithography), adhesives (both conductive and non conductive for die attach and assembly interconnects), interlayer dielectrics(low k, low loss dielectrics for high speed and low loss signal transmission), encapsulants(discrete and wafer level packages for device protection) , embedded passives(high K, capacitors, high Q ,inductors for high density PWB substrates), superhydrophobic self-cleaning lotus effect surfaces,...etc. In this presentation, I will review some of the recent advances on polymeric materials and polymer nanocomposites that are currently being investigated for these types of applications, such as : lead-free electrically conductive adhesives (ECAs) with self assembly monolayer molecular wires for fine pitch and high current density interconnects, flip chip and wafer level underfills, nano lead-free alloys for low temperature interconnects, nanometal particle composites for high k embedded passives, well-aligned carbon nanotubes and graphenes for high current and high thermal interface materials(TIMs), and superhydrophobic self-clean lotus surface coatings for high efficiency solar cell applications.

Spin-based MOSFET and its applications

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A spin metal-oxide-semiconductor field-effect transistor (spin MOSFET) is a promising candidate for extended complementary metal-oxide semiconductor (CMOS) devices. Up to now, the spin-dependent transport through semiconductor channels, which is essential to realize the spin MOSFET, has been observed by using non-local and Hanle effect measurement methods. Recently, we succeeded in observing the spin-dependent transport through Si with local measurement configuration due to reduction in the contact resistance in ferromagnetic metal (FM) /thin insulator tunnel barrier (I)/Si junctions [1-3]. Towards practical application, we also proposed a novel spin-based MOSFET Spin-Transfer-torque-Switching MOSFET (STS-MOSFET) which offers non-volatile memory and transistor functions that are CMOS compatible and have high endurance and a fast write time. STS-MOSFETs with Heusler alloy (Co2FeAl0.5Si0.5) were prepared and reconfigurability of the novel spintronics-based STS-MOSFET was successfully realized in the transport properties. The device showed magnetocurrent (MC) and write characteristics with an endurance of over 100000 cycles. The overall properties of the STS-MOSFETs show promising potential for future reconfigurable integrated circuits based on CMOS technology. It was also clarified that the read characteristic can be improved in terms of MC ratio; however, it is deteriorated in terms of mobility by choosing connection configurations of the source and drain in the STS-MOSFETs. Moreover, large scale circuit simulations for various field programmable gate arrays (FPGAs) [4] revealed that the critical path delay is significantly improved by using the STS-MOSFETs. The overall properties of the STS-MOSFETs show great potential for future reconfigurable integrated circuits based on CMOS technology.

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Flexible thin film transistor arrays as an enabling platform technology: Opportunities and challenges

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The tremendous successful of the flat panel display industry can in large part be attributed to the industry's ability to manufacture high quality large area thin film transistor (TFT) arrays on glass substrates at high yield and throughput. Intensive strategic efforts over the past decade to develop new processes and materials for manufacturing TFT arrays on flexible plastic or metal foil substrates is pushing us to the dawn of a flexible display industry. In this paper we take a speculative look into the future, with the basic premise that the ready manufacture of large area flexible TFT arrays will provide a tremendous opportunity to create not just flexible displays, but revolutionary transformational engineered products and systems with unique and desirable form, fit and function. In these macroTechnology systems, materials and nano-, micro-, and macro-scale devices are integrated to produce valuable multi-functional products that are characteristically thin, lightweight, flexible, conformable, and ultra-rugged for use under challenging conditions. The practical opportunities seem limitless: one can envision+ new dual-use technologies that can be deployed to address critical needs in a diverse application space from health sciences to information and decision technology, security and emergency response, transportation, energy and the environment.

To realize the full promise of flexible systems technology, fundamental and technical challenges in two critical areas must be addressed:
-Flex-compatible Functional Materials and Nanostructures -- high-performance, low-temperature TFTs and circuits along with critical transparent conductors and environmental barriers for energy harvesting, sensing, actuation, memory and wireless communication.

-Scaleable and Sustainable Manufacturing -- low temperature flex-compatible processes, flexible substrate handling protocols, novel additive and other environmentally-benign processing.

With an emphasis on TFT materials, devices and processes, this paper will summarize the ongoing efforts to effectively address these challenges. We will also highlight the R&D opportunities defined by the remaining principal technology gaps.

Vertical channel thin film transistor: Improvement approach similar to multigate monolithic CMOS technology

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The silicon based thin film transistors (TFTs) technological process evolution is governed by electrical performance improvements that are needed for the numerous fields of large area electronic applications. The main objective is to fabricate TFTs at a temperature low enough to be compatible with the substrates, such as glass substrates, integrated circuit processed substrates (above IC devices), and flexible substrates, that implies several approaches with good enough electrical properties. Previous papers highlighted the influence of the process and the quality and the nature of the channel material on the electrical properties of the TFTs, mainly equivalent mobility of carriers in the channel, Ion/Ioff drain current ratio, and subthreshold slope. The previous studies also involved as well planar processes that means channel parallel to the substrate surface as quasi-vertical channel, source, channel and drain region being stacked. This last choice allows an increase of the equivalent current density flowing in the circuit thanks to the two modifications, the channel length that can be much shorter and the channel width that can be much higher, for the same design rules. However, the leakage current between drain and source was observed as directly dependent of the face-to-face common area between source and drain, while Ion is proportional to channel width. This behavior was also observed in vertical monolithic structures such as multigate MOSFET and FinFET. To minimize this leakage current that affects drastically the Ion/Ioff ratio, a first way consists to decrease the geometry, in this case the distance between the two vertical channels. This means an improvement of the alignment techniques that is difficult to insure due to the relatively high thicknesses of the films. The second way consists to include an insulator between source and drain, the channel region being deposited just on the quasi vertical sidewalls. The recent studies were oriented on this solution. After the presentation of the interest of such vertical channel structures on both thin film and ULSI technologies, a review on the different solutions already proposed is given and discussed. These approaches are thus similar to ones applied to CMOS monolithic silicon technology involving vertical channels.

Low power 6.0-Inch extended graphics array reflective liquid crystal display using crystalline indium gallium zinc oxide semiconductor with electronic paper function

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Electronic paper displays have become available on the market as novel thin display devices. In electronic paper displays, electrophoresis elements are often used, because they have memory functionality and the driving number of drivers can be significantly reduced. Consequently, power consumption can be markedly reduced. Further, electrophoretic displays have the following advantages: texture like paper, high visibility, and applicability to flexible displays. Thus, electrophoretic displays have been widely used. However, the electronic paper displays have problems as follows: high drive voltage of drivers needed for rewriting data, insufficiency of colorization and expression of gray levels, long rewrite time due to low response speed, difficulty of displaying moving images, and high cost. In particular, the low response speed is a major problem because operability is impaired.

We focus on the ultra-low leakage current of IGZO TFTs. The power consumption of an LCD panel can be markedly reduced by significantly lowering frame frequency, i.e., stopping unnecessary rewrites at the time of displaying still images. Accordingly, our LCD panel can be applied to an electronic paper display.

We succeeded in fabricating 6.0-in. XGA reflective LCD. We proved that the interval between rewrites of data to pixels could be extended to 3 min (1/180 fps). The power consumption at the time of displaying images at 1/180 fps is approximately 1/10000 the power consumption at 60 fps. In the case of displaying monochrome (B/W) still images such as documents, the interval between rewrites can be further extended in terms of visibility. If the power consumption can be reduced to this extent, our LCD panel will be applicable not only to the sub displays of cellular phones but also to electronic paper displays.

Biosensors based on organic thin film transistors

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Organic thin film transistors (OTFT) have been successfully used in various types of biosensors and show many advantages, such as easy fabrication, low cost, biocompatibility, high sensitivity and flexibility. In this paper, we will report the following sensors based on organic electrochemical transistors, including DNA sensor, glucose sensor, dopamine sensor and cell-based biosensor. All of this sensors show promising performance and suitable for real applications. (1) A novel label-free DNA sensor has been realized by using an OTFT integrated in a microfluidic system. Single-stranded probe DNA is immobilized on the surface of the Au gate electrode of the OTFT. The sensor can be used to detect the target complementary DNA down to 10 pM. (2) OTFTs with glucose oxidase-modified Pt gate electrodes are successfully used as highly sensitive glucose sensors. The gate electrodes are modified with nanomaterials (multi-wall carbon nanotubes or Pt nanoparticles), which results in a dramatic improvement in the sensitivity of the devices. The detection limit of the device modified with Pt nanoparticles is about 5nM, which is three orders of magnitude better than a device without the modification. (3) OTFTs with different gate electrodes, including graphite, Au and Pt electrode etc., have been used as dopamine sensor for the first time. We find that the device with a Pt gate electrode characterized at the gate voltage of 0.6V shows the highest sensitivity. The detection limit of the device to dopamine is 0.5nM, which is two orders of magnitude better than a conventional electrochemical measurement with the same Pt electrode. (4) Cell-based biosensors with cells cultivated on top of the devices have been studied. The activities of the cells under the effect of drugs have been monitored by characterizing the OTFTs. It has been found that the performance of the device is sensitive to the surface charge and the morphology of the attached cells due to the electrostatic interaction between the adherent cells and the active layer of the OTFTs. The devices are suitable for applications in disposable and label-free cell-based biosensors for high throughput sensing.

MILC PMOS poly-silicon TFT circuits and application in SOP

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Research towards thin film circuits is one of the most attractive directions of the large-area electronics and flexible electronics. The poly-Si TFT technology is used for commercialization in active matrix display. P-type metal induced lateral crystallization is a promising technology to realize high performance poly-Si TFT. However, due to the intrinsic grain boundaries of Poly-Silicon causing a negative effect on device performance such as mobility and uniformity, there is always much difficulty and little progress to realize high performance circuits using such simplified process.

In this work, the research on TFT shift register circuit which is critical for system integration on panel is presented. The whole circuit is made up of MILC PMOS Poly-Si TFTs. The TFT device exhibited field-effect mobility of 65.21cm2/Vs, threshold voltage of -3.5V and sub-threshold swing of 0.56V/dec. Some special design considerations were adopted to improve the robustness of the circuits. The whole shift register is composed of as many as 180 stages and exhibited well with frame frequency from 22Hz to 220Hz at the power supply voltage of 11V. The rising and falling time of each output could be less than 8us and 2us respectively. No deduction and distortion appeared from the first to the final stage. On the other hand, the effect of bootstrapping and dynamic behavior in circuits is analyzed. The fabrication and reliability analysis of the PMOS TFT shift register circuit are also discussed in this paper. In conclusion, the high performance driver circuits based on our MILC PMOS process are possible and have the potential in the application of SOP electronics.